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HDLC data link for cellular radio systems - uses embedded bits
replacing all ones sequence to transport clocking synchronisation
information to remote sites

MOTOROLA INC 27.02.90-US-486468

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The data link arranges an HDLC data link to transport a special
class of data (such as synchronization or other signalling
information), in addition to the normal data transported. At the
sending end of the link the all-1's sequence corresponding to the idle
sequence between individual HDLC packets is detected.

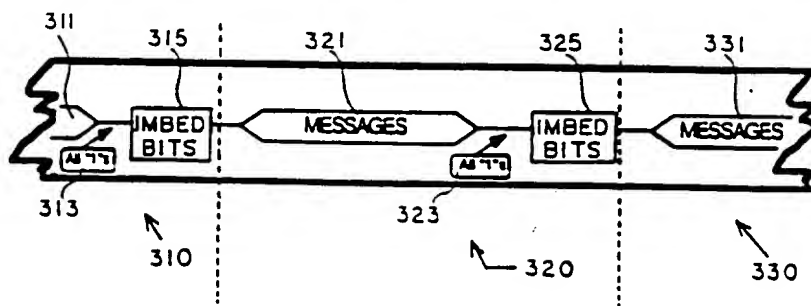
Once eight (8) consecutive 1's are detected, a desired number of
1's is removed and a like number of synchronization bits are inserted
(or embedded) in their place, at the receiving end of the link the
inserted synchronization bits are detected, and removed from the
idle sequence.

ADVANTAGE - Each data link transports synchronization
information along with data information, so reducing the number of
e.g. linking facilities needed. (12pp Dwg.No.3/0)

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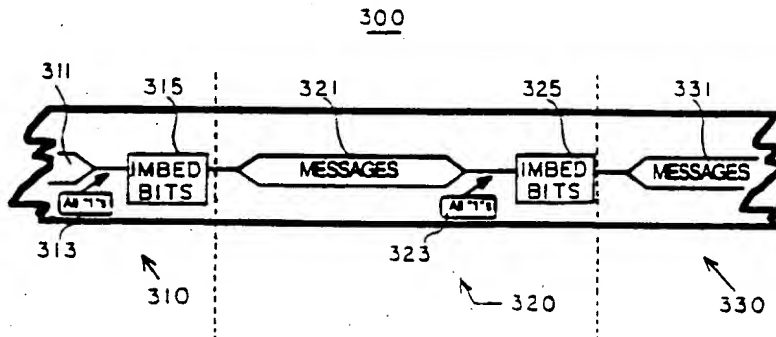
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(54) Data link with an imbedded channel.

(57) A method and apparatus for arranging an HDLC data link to transport a special class of data such as, for example, synchronization or other signalling information, in addition to the normal data transported by the data link is provided. According to the invention, at the sending end of the link the all-1's sequence corresponding to the idle sequence between individual HDLC packets is detected. Once eight (8) consecutive 1's are detected, a desired number of 1's is removed and a like number of synchronization bits are inserted in their place. At the receiving end of the link the inserted synchronization bits are detected, removed, and a like number of 1's inserted in their place.



EP 0 444 832 A2

Technical Field

This application relates to clocking techniques that may be used in cellular radio infrastructure systems and more particular to a method of imbedding an additional channel in an data communications link
 5 compliant with the High Level Data Link Control (HDLC) protocol.

Background of the Invention

RF communication systems having a plurality of transmitter sites are well known. An example of such a
 10 system, of course, is a cellular radio system. Such a system is depicted in Fig. 1. There is shown a cellular radio system 100 having a plurality of transmitter sites, as in the prior art. Although Fig. 1 only depicts two such transmitter sites, 111 and 131, it will be appreciated that the actual number of sites will vary from system to system.

Referring now to transmitter site 111, a common base station 105 is coupled to a digital radio interface
 15 module 115 via link 113. The digital radio interface module 115, in turn, is coupled to a radio control unit module 119 via link 117. The radio control unit module 119, in turn, is coupled to an antenna 121.

Referring now to transmitter site 131, the common base station 105 is coupled to a digital radio
 interface module 135 via link 133. The digital radio interface module 135, in turn, is coupled to a radio
 control unit module 139 via link 137. The radio control unit module 139, in turn, is coupled to an antenna
 20 141.

Typically the links 117 and 137 are implemented using fiber optic cables. Also, typically these links are arranged as ISO layer 2 HDLC data links.

Referring still to Fig. 1, those skilled in the art will appreciate that the remote radio control unit modules
 119 and 139 must be synchronized to a common clocking source in the common base station 105. There
 25 are several ways to distribute clocking information to the remote sites. One way would be to run additional fiber optic facilities from the serving digital radio interface modules. The problem with this approach is the added cost for providing the additional fiber optic link for each transmitter site. Considering the length of each link and the total number of sites, this approach may prove expensive.

As a result, it would be desirable to arrange each individual data link to transport the needed
 30 synchronization information along with the data information transported by the HDLC protocol.

Summary of the Invention

It is an object of the invention, therefore, to provide a method for a channel to send and receive
 35 imbedded bits. These imbedded bits are arranged to transport further information in addition to the data transported by the data link protocol that is running on the channel.

Therefore, a data link with an imbedded channel, according to the invention, is disclosed. At the
 sending end of the link, an all-1's pattern corresponding to the idle sequence between successive HDLC-
 type frames is detected. Once a predetermined number of 1's are detected, a desired number of bits are
 40 encoded and inserted (or imbedded) into the idle bit sequence. The imbedded bits may be utilized to transport additional information such as, for example, control, signalling, timing, synchronization, data, text, or other information. At the receiving end of the link, the imbedded bits are detected and recovered from the idle sequence.

Brief Description of the Drawings

Fig. 1 shows an RF communication system having a plurality of transmitter sites, as in the prior art.

Fig. 2 shows a typical HDLC frame format, as in the prior art.

Fig. 3 is a timing diagram depicting a first embodiment of a data link with an imbedded channel,
 50 according to the invention.

Fig. 4 is a block diagram depicting a further embodiment of the invention.

Figs. 5A and 5B are flow diagrams depicting a further embodiment of the invention.

Fig. 6 is a block diagram depicting a further embodiment of the invention.

Detailed Description of the Invention

As above, the channel interconnecting the digital radio interface and the radio control unit has an HDLC-
 type data link implemented on it. The frame format of the HDLC protocol is well-known and is shown in Fig

2. The header and trailer are the standard HDLC opening and closing flags and operate in the non-shared mode. The information field contains a message type, a message number, and the message to be transported by the frame. As is known, the idle time between messages is filled with a predetermined idling sequence comprising "all ones" or "all 1's".

5 In addition to the data contained in the HDLC frame, the applicant has discovered that the digital radio interface may be arranged to transmit other information to the radio control unit via this channel by encoding and sending embedded bits during the idle sequence that occurs between successive HDLC frames.

10 In particular, the applicant has discovered that the digital radio interface may utilize the foregoing technique to transport synchronization or timing information to the radio control unit. In what follows, therefore, it will be assumed that the imbedded bits are used to transport such timing or synchronization signals. Those skilled in the art will appreciate, however, that the invention is equally applicable in applications where the imbedded information sought to be transported relates to other purposes such as, for example, control, signalling, data, text, or still other uses.

15 To achieve proper synchronization, therefore, the data radio interface encodes a predetermined bit pattern and transmits it to the radio control unit via the link. This timing information is transmitted during the link idle time after the last set of messages have been transmitted but before the next set of messages is transmitted. This timing information is not framed by the HDLC opening/closing flags, and is therefore ignored by the HDLC receiver. This is illustrated in Fig. 3.

20 In Fig. 3 there is shown a time sequence of three consecutive frames comprising a previous frame 310, a current frame 320, and a next (or following) frame 330.

Looking now at the current frame 320, note that after all current messages 321 have terminated, the channel reverts to an "all 1's" sequence 323. It is during this condition 323 that the imbedded bits (designated "IMBED BITS") 325 carrying the timing information are inserted.

25 The previous frame 310 and the next frame 330 exhibit a similar pattern. For instance, note that the previous frame 310 contains several imbedded bits 315 that follow an "all 1's" sequence 313. Similarly, it may be assumed that the next frame 330 also contains a sequence of imbedded bits, although this is not shown.

30 Referring still to Fig. 3, each imbedded bit sequence conveys a timing signal or mark used for synchronizing the corresponding frame. In the current system, seven individual timing marks are used. As a result, seven individual bit patterns are required. The correspondence of the imbedded bit patterns to the seven timing signals is shown in Table 1, below:

TABLE 1

| Information | Imbedded Bit Pattern |
|---------------|----------------------|
| Timing Mark 1 | 11111111000011111111 |
| Timing Mark 2 | 11111111000111111111 |
| Timing Mark 3 | 11111111001011111111 |
| Timing Mark 4 | 11111111001111111111 |
| Timing Mark 5 | 11111111010011111111 |
| Timing Mark 6 | 11111111010111111111 |
| Timing Mark 7 | 11111111011011111111 |

These bit patterns are chosen to assure that the HDLC receiver will not mistake the synchronization information for an opening flag, closing flag, or data corresponding to the HDLC frame structure of Fig. 2. Those skilled in the art will appreciate that, since the HDLC protocol is utilized as the link-level data transmission format, it is guaranteed that the bit patterns in Table 1 above will never appear in the HDLC data stream. This arrangement, therefore, eliminates the need for any type of receive gate or "window" through which to detect or "watch for" the timing mark.

Fig. 4 shows a digital radio interface module 410 coupled to a remote radio control unit module 450 via a fiber optic cable 440.

The module 410 accepts the data input 413 and the timing input 411 from the common base station electronics, such as that depicted as 105 in Fig. 1. The data is converted into an HDLC format 419 via the HDLC transmitter 415. The synchronized timing information 411 is converted into its transmission format 421 (as per Table 1) via the timing mark generator 417. This information is then combined through a multiplexer 425 and applied to a manchester encoder 427 which supplies the fiber optic transmitter 431 which, in turn, drives the fiber optic cable 440.

At the receiving end of cable 440, the signal is received by fiber optic receiver 451 which is coupled to a manchester decoder 453. The decoder 453's output 455 is split into two branches 457 and 459. Branch 457 is input to an HDLC receiver 461, and branch 459 is input to timing mark decoder 463.

Referring still to module 450, the HDLC receiver 461 scans its input bit stream 457 for opening flags. When one is found, it converts the following bits from the HDLC frames to the user output data stream 465. In parallel with the foregoing HDLC decoding process, the timing mark decoder 463 also scans its input bit stream 459 for timing information, as per Table 1.

Fig. 5A depicts a flow diagram for an encoding process. The process begins at step 501, and then proceeds to step 503, where it determines whether the HDLC closing flag for the last message in the current frame has been sent. If the flag has not been sent (corresponding to a negative determination for step 503), then the process waits until the flag is sent (corresponding to a positive determination for step 503).

Once the closing flag has been sent, the process proceeds to step 505. Here it determines whether at least eight (8) consecutive 1's have been sent. If at least eight (8) consecutive 1's have not been sent (corresponding to a negative determination for step 505), then the process waits until at least eight (8) consecutive 1's have been sent (corresponding to a positive determination for step 505).

Once at least eight (8) consecutive 1's have been sent, the process proceeds to step 507. Here it removes a predetermined number of 1's and inserts (or imbeds) a like number of synchronization bits. As mentioned above, it will be appreciated that the inserted bits may be used to transport other information, as well, such as signalling or control information.

The bit pattern of the imbedded bits may vary from application to application. Some valid bit patterns are given, for example, in Table 1 above. In encoding the imbedded message bits, however, care must be exercised to avoid inadvertently generating the HDLC "flag" pattern, 01111110. The reason for this, of course, is that this bit pattern would cause the HDLC receiver to erroneously interpret the imbedded message as the beginning of the next HDLC message.

After the desired message bits have been imbedded, the encoding process is complete for the current frame. As a result, the process returns (step 509) to step 501, where it waits for the next frame.

Fig. 5B depicts a flow diagram for a decoding process. The process begins at step 551, and then proceeds to step 553, where it determines whether the HDLC closing flag for the last message in the current frame has been received. If the flag has not been received (corresponding to a negative determination for step 553), then the process waits until the flag is received (corresponding to a positive determination for step 553).

Once the closing flag has been received, the process proceeds to step 555. Here it determines whether at least eight (8) consecutive 1's have been received. If at least eight (8) consecutive 1's have not been received (corresponding to a negative determination for step 555), then the process waits until at least eight (8) consecutive 1's have been sent (corresponding to a positive determination for step 555).

Once at least eight (8) consecutive 1's have been received, the process proceeds to step 557. Here it detects and decodes the imbedded message bits. After the desired message bits have been decoded, the decoding process is complete for the current frame. As a result, the process returns (step 559) to step 551, where it waits for the next frame.

As before, other methods for accomplishing synchronization generally have required a receive gate or "window" to be opened when the timing information is expected, since its timing mark may occur anywhere in the data stream. Therefore, one benefit of a data link with an imbedded channel, according to the invention, is that no receive gate or "window" is required since the timing mark bit pattern cannot occur in

the HDLC formatted stream.

Referring now to Fig. 5 there is shown a communications system 600 including four remote transmitter sites. There is shown a common base station equipment 501 including four digital radio interface modules 603, 605, 607, and 609. As shown, each digital radio interface module (603, 605, 607, and 609) drives a channel (615, 617, 619, and 621) coupled to a remote radio control unit module (625, 627, 629, and 631). Also as shown, each radio control unit module (625, 627, 629, and 631) drives an antenna (635, 637, 639, and 641). It will be appreciated that each radio interface module and its corresponding radio control module may be equipped with apparatus similar to Fig. 4.

In accordance with the invention, each radio control unit receives its data and timing information over a single fiber optic link. Since the radio interface modules and radio control modules may be replicated and all radio interface modules (603, 605, 607, and 609) are connected to a common timing reference in the common base station equipment 601, then all radio control units (625, 627, 629, and 631) are thus synchronized.

A further capability of a data link with an imbedded channel, according to the invention, is the ability to utilize the timing marks for control. For example, several of the timing marks of Table 1 may be reserved to implement device-specific control functions. For example, a first mark may be a command to place the radio control unit in a sleep mode to conserve power, while a second mark may be a wake-up command for bringing the radio control unit back on-line when it is needed by the system.

While various embodiments of a data link with an imbedded channel, according to the present invention, have been described hereinabove, the scope of the invention is defined by the following claims.

Claims

1. A receiver for receiving imbedded characters on a channel having a data link implemented thereon using a protocol that receives a message, and where said channel receives idle characters after a message has been received, said receiver comprising:
 - message determining means for determining when a message has been received;
 - idle determining means responsive to said message determining means for determining when at least a predetermined number of idle characters have been received; and,
 - means responsive to said idle determining means for receiving at least one imbedded character.
2. The receiver of claim 1 where said message contains a flag and said at least one imbedded character is based at least in part on said flag.
3. A receiver for receiving imbedded bits on a channel that is arranged to receive frames, the channel being further arranged to receive an idle pattern of "all 1's" after each frame, said receiver comprising:
 - frame determining means for determining when a frame has been received;
 - idle determining means responsive to said frame determining means for determining when at least a predetermined number of "1's" have been received; and,
 - means responsive to said idle determining means for receiving at least one imbedded bit.
4. The receiver of claim 3 where said frames include a beginning bit pattern and said at least one imbedded bit is based at least in part on said beginning bit pattern.
5. A radio control unit module including a receiver for receiving imbedded characters on a channel having a data link implemented thereon using a protocol that receives a message, and where said channel receives idle characters after a message has been received, said receiver comprising:
 - message determining means for determining when a message has been received;
 - idle determining means responsive to said message determining means for determining when at least a predetermined number of idle characters have been received; and,
 - means responsive to said idle determining means for receiving at least one imbedded character.
6. The radio control unit module of claim 5 where said message contains a flag and said at least one imbedded character is based at least in part on said flag.
7. A receiver for receiving imbedded characters on a channel having a data link implemented thereon using a protocol that receives a message, and where said channel receives a stream of idle characters after a message has been received, said receiver comprising:

a decoder arranged for detecting that a message has been received;

said decoder further arranged for detecting, after said message has been received, that at least a predetermined number of idle characters have been received; and,

said decoder further arranged for detecting, after said at least a predetermined number of idle characters have been received, the presence of at least one imbedded character in said stream of idle characters.

8. The receiver of claim 7 where said message contains a flag and said at least one imbedded character is based at least in part on said flag.

9. A cellular radio telephone base station including a receiver for receiving imbedded characters on a channel having a data link implemented thereon using a protocol that receives a message, and where said channel receives idle characters after a message has been received, said receiver comprising:

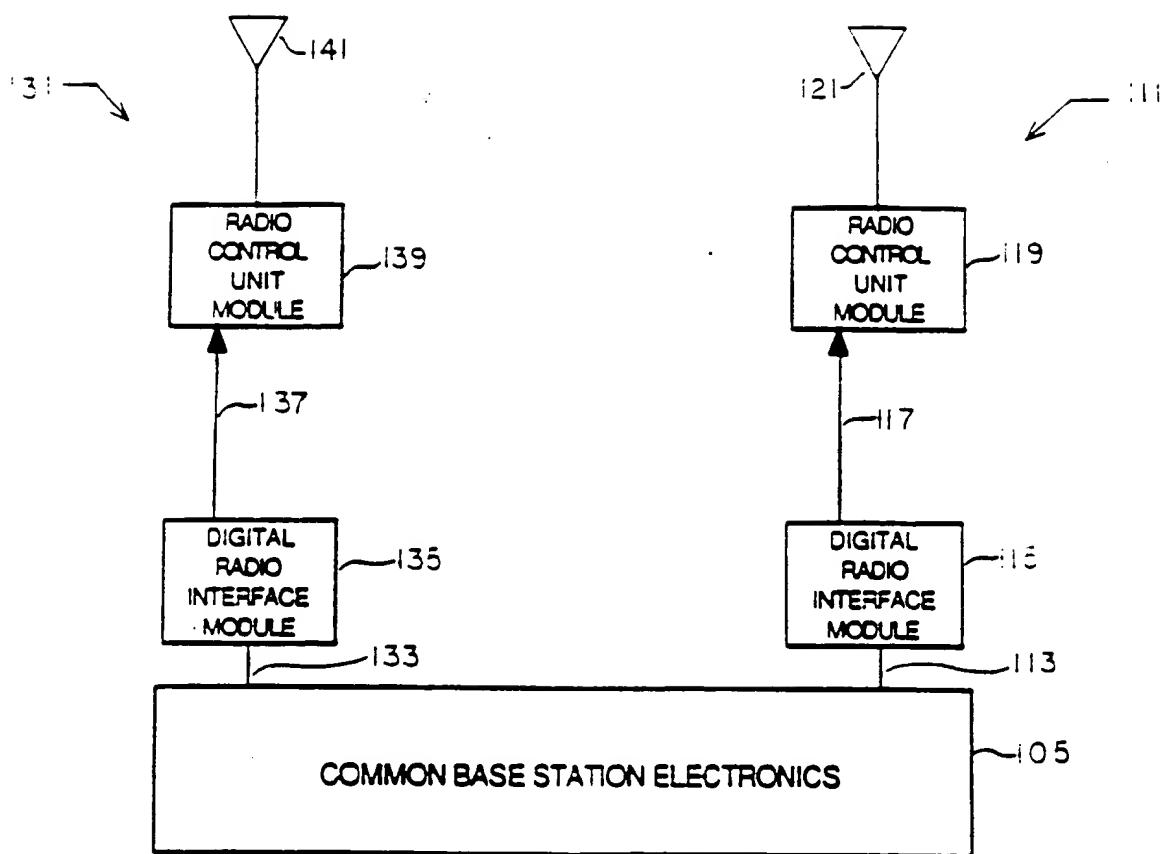
message determining means for determining when a message has been received;

idle determining means responsive to said message determining means for determining when at least a predetermined number of idle characters have been received; and,

means responsive to said idle determining means for receiving at least one imbedded character.

10. The cellular radio telephone base station of claim 9 where said message contains a flag and said at least one imbedded character is based at least in part on said flag.

100



(PRIOR ART)

FIG. 1

200 (PRIOR ART)

| HEADER | INFORMATION | | | ERROR CHECK | TRAILER |
|--------------|--------------|----------------|------------|----------------------|--------------|
| Opening Flag | Message Type | Message Number | Message | Frame Check Sequence | Closing Flag |
| 01111110 | 8 Bits | 8 Bits | n x 8 Bits | CRC 16 Bits | 01111110 |

FIG. 2

300

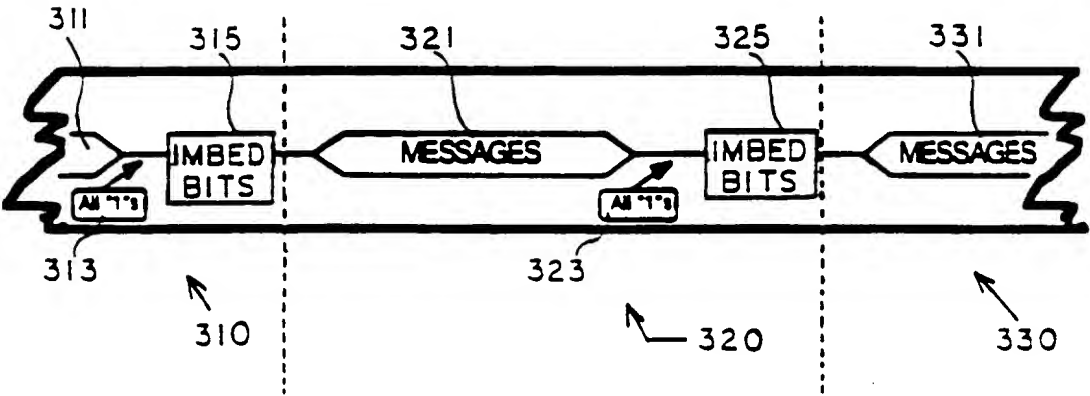


FIG. 3

400

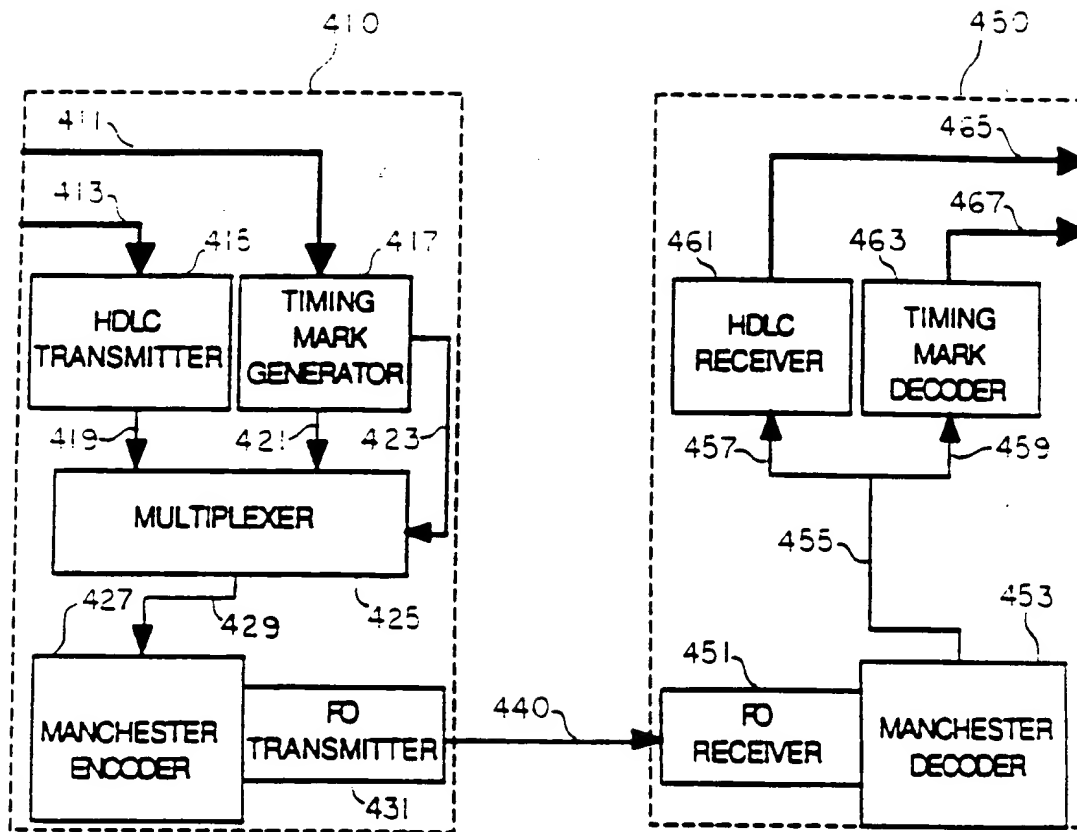


FIG. 4

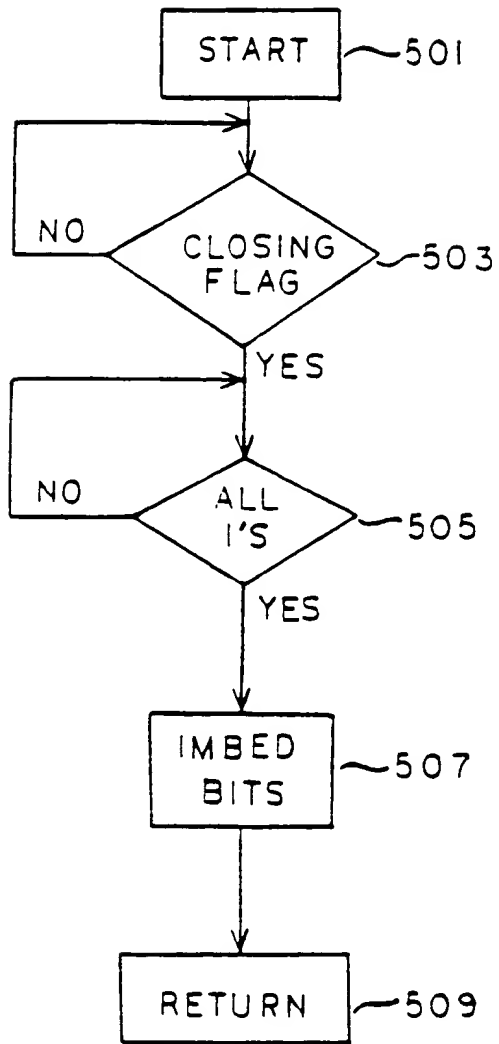


FIG. 5A

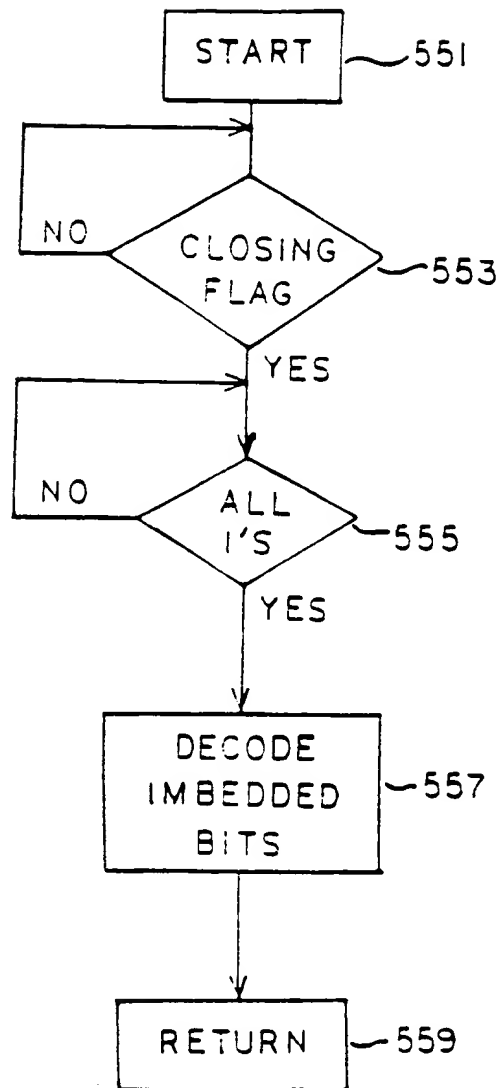


FIG. 5B

600

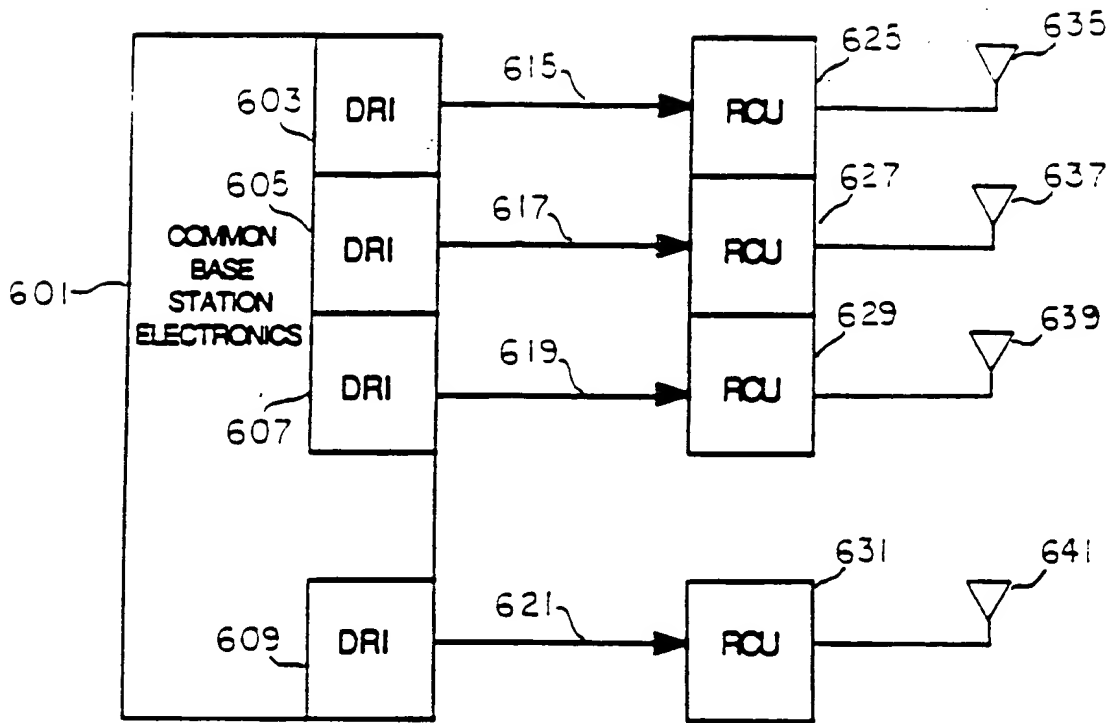


FIG. 6